TevBPM Upgrade Hardware Meeting, November 6, 2003

Present: Jim Steimel, Vince Pavlicek, Luciano Piccoli, Dehong Zhang, Stephen Wolbers, Rob Kutschke, Bob Webber

Main Topic: Digital Signal Receiver (DSR) and its applicability for the Tevatron BPM

Brian Chase was not able to make the meeting. Therefore, some of the discussion was not "authoritative" and Jim will track Brian down to get answers to some of the questions.

Some of the questions posed include:

- Will the system handle 47 KHz data rate?
- Can the system synchronize with the beam?
- What is the format of the design files? (probably pCAD)

There was a great deal of discussion about the DSR and how it would be used for the Tevatron BPM. One question that arose is how much time a modification to the board (newer DSP, DSP with more memory, added FPGA, etc.) would add to the investigation. A DSP with more memory is probably pin-for-pin compatible and would require no changes to the board. Very small changes, such as adding a couple of traces for extra address lines or triggers, could be handled by Brian's group in a couple of days. Any more substantial changes to the achitechture would probably take on the order of a month (or more).

Some action items:

- Jim will talk to Brian to get answers to some of the questions that he has about the ability of this board to satisfy the Tev BPM measurements.

- Mark Bowden is continuing his investigation of the

Echotek board, including getting quotes for price and delivery schedule.

- We talked about the possibility of getting our hands on a crate and a DSR card to test.

We will next meet on Monday, November 10 at 11:00.